AMENDMENTS TO THE CLAIMS:

This listing of claims will replace all prior versions and listings of claims in the application:

1. (Currently Amended) An encoder comprising:

filtering generation means ~~which generates~~ for generating a filtering coefficient by performing a filtering process ~~processing~~ on inputted picture data;

division means ~~which divides~~ for dividing the filtering coefficient into plural bit planes from an uppermost bit to a lowermost bit of each pixel;

read control means ~~which removes~~ for removing a predetermined number of bit planes among the ~~plural~~ bit planes, from a lower side, thereafter reads remaining bit planes, and outputs the remaining bit planes in parallel; and

~~plural~~ a plurality of encoding means ~~which respectively perform~~ for encoding ~~processings on the plural~~ the bit planes outputted in parallel from the read control means, wherein

the read control means determines the predetermined number of the removed bit planes, so that a quantity of generated codes per frame is kept constant when each of the ~~plural~~ encoding means performs the encoding ~~processing~~.

2. (Currently Amended) The encoder according to claim 1, wherein

the read control means removes the first quantity ~~predetermined number~~ of bit planes, from the lower side and from a lower hierarchical level, from bit planes stored in storage means.

3. (Currently Amended) The encoder according to claim 1, further comprising

rate control means for ~~which performs~~ feeding forward in order that the second quantity of generated codes per frame is kept constant, based on results of the encoding process ~~processings~~ of the plural encoding means.

4. (Currently Amended) An encoding method comprising:

~~a first step of~~ generating a filtering coefficient by performing a filtering process ~~processing~~ on inputted picture data;

~~a second step of~~ dividing the filtering coefficient into plural bit planes from an uppermost bit to a lowermost bit of each pixel;

~~a third step of~~ removing a predetermined number of bit planes among the plural bit planes, from a lower side, thereafter reading the remaining bit planes, and outputting the remaining bit planes in parallel; and

~~a fourth step of performing~~ encoding ~~processings respectively on the plural~~ the bit planes outputted in parallel, wherein

the predetermined number of the removed bit planes is determined in the removing ~~third~~ step so that a quantity of generated codes per frame is kept constant when ~~the~~ encoding the bit planes. ~~processings are performed in the fourth step.~~

5. (Currently Amended) The encoding method according to claim 4, wherein,

~~in the third step,~~ removing the predetermined number of bit planes comprises removing the predetermined number of bit planes ~~is removed from the bit planes,~~ from the lower side and from a lower hierarchical level.

6. (Currently Amended) The encoding method according to claim 4, further comprising

~~a sixth step of~~ setting the predetermined number of bit planes removed in the removing ~~removed in the third~~ step, which is necessary to keep the quantity of generated codes per frame constant, based on results of the performed encoding processing ~~processings in the fourth step~~, and thereafter feeding back the predetermined number to the ~~third~~ removing step.

7. (New) An encoder, comprising:

a video input section for receiving picture data and separating the picture data into data components;

a wavelet converter for receiving the data components from the video input section and dividing the data components into frequency components;

a quantizer for quatizing the frequency components received from the wavelet converter;

a bit plane converter for receiving the quantized frequency components supplied from the quantizer and dividing the quantized frequency components into code blocks, the bit plane converter further dividing the code blocks into a plurality of bit planes;

a rate controller for performing a rate control so that only necessary bit planes are sent to a register;

a plurality of bit model sections, each bit model section receiving a corresponding one of the necessary bit planes from the register and creating a context based on the received necessary bit plane;

a plurality of arithmetic encoders, each arithmetic encoder performing an entropy encoding and calculating generation probabilities for the context to create encoded streams; and

a format generator for rearranging the encoded streams and adding additional information to the encoded streams to create data streams, the format generator outputting the data streams.

8. (New) The encoder of claim 7, wherein the rate controller removes a predetermined quantity of bit planes among the bit planes to obtain the necessary bit planes.

9. (New) The encoder of claim 8, wherein the predetermined quantity of bit planes is determined such that the arithmetic encoders encode substantially the same amount of generated codes.